

AMENDED CLAIM SET:

1 1. (currently amended) A field effect device having a gate dielectric and a channel region,
2 wherein the gate dielectric comprises a germanate material layer and an interlayer
3 disposed between the channel region and the germanate material layer, wherein the
4 interlayer is oxide or oxynitride.

1 2. (canceled)

1 3. (currently amended) The field effect device of claim 2 1, wherein the germanate
2 material layer has a dielectric constant over 4.

1 4. (original) The field effect device of claim 3, wherein the germanate material layer has
2 a dielectric constant approximately between 8 and 40.

1 5. (currently amended) The field effect device of claim 2 1, wherein the germanate
2 material layer has a thickness of approximately between 1.5nm and 50nm.

1 6. (canceled)

1 7. (currently amended) The field effect device of claim ~~6~~ 1, wherein the interlayer is less
2 than approximately 1nm thick.

1 8. (canceled)

1 9. (currently amended) The field effect device of claim 1, wherein the gate dielectric
2 comprising the germanate material layer possesses greater resistance against charge
3 tunneling than a SiO₂ gate dielectric, and a capacitance per unit area of the gate dielectric
4 comprising the germanate material layer is at least as large as the capacitance per unit
5 area of the SiO₂ gate dielectric.

1 10. (currently amended) The field effect device of claim 1, wherein the germanate
2 material layer is hafnium germanium oxide layer.

1 11. (original) The field effect device of claim 1, wherein the field effect device is a Si
2 MOS transistor.

1 12. (original) The field effect device of claim 1, wherein the field effect device is a SiGe-
2 based MOS transistor.

1 13. (original) The field effect device of claim 1, wherein the field effect device is a Ge.
2 MOS transistor.

1 14. (original) The field effect device of claim 1, wherein the field effect device is a III-V
2 material based MOS transistor.

1 15. - 25. (canceled)

1 26. (currently amended) A processor, comprising:
2 at least one chip, wherein the chip comprises at least one semiconductor field
3 effect device having a gate dielectric and a channel region, wherein the gate dielectric
4 comprises a germanate material layer and an interlayer disposed between the channel
5 region and the germanate material layer, wherein the interlayer is oxide or oxynitride.

1 27. (original) The processor of claim 26, wherein the processor is a digital processor.

1 28. (original) The processor of claim 26, wherein the processor comprises at least one
2 analog circuit.